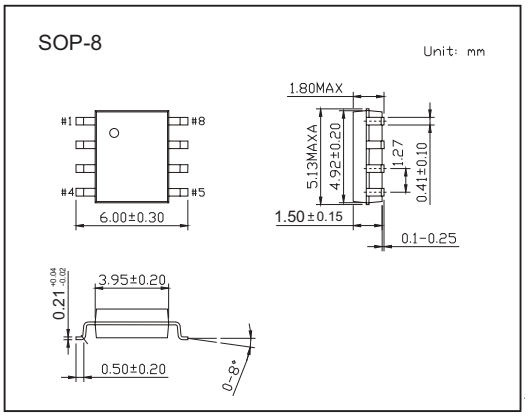
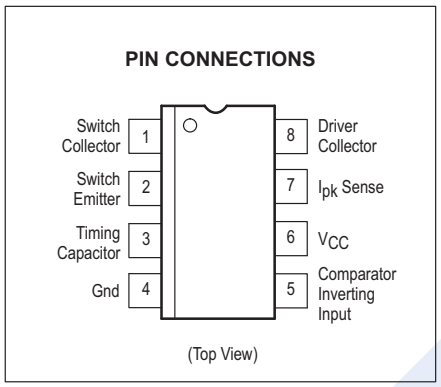
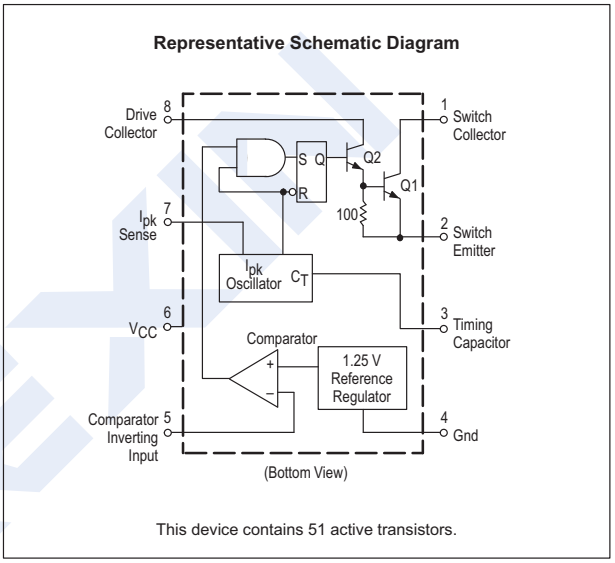
DC-to-DC Converter Control Circuits
KM34064



■ Features

- Operation from 3.0 V to 40 V Input
- Low Standby Current
- Current Limiting
- Output Switch Current to 1.2 A
- Output Voltage Adjustable
- Frequency Operation to 100 kHz
- Precision 2% Reference





■ Absolute Maximum Ratings Ta = 25℃

Parameter	Symbol	Rating	Unit
Power Supply Voltage	V_{CC}	40	V
Comparator Input Voltage Range	V_{IR}	-0.3 to +40	
Switch Collector Voltage	$V_{C(switch)}$	40	
Switch Emitter Voltage (VPin 1 = 40 V)	$V_{E(switch)}$	40	
Switch Collector to Emitter Voltage	$V_{CE(switch)}$	40	
Driver Collector Voltage	$V_{C(driver)}$	40	
Driver Collector Current (Note 1)	$I_{C(driver)}$	100	mA
Switch Current	I_{SW}	1.2	A
SOP8 Package, D Suffix TA = 25°C	P_D	625	mW
Thermal Resistance	$R_{\theta JA}$	160	°C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature Range	T_A	0 to+70	°C
Storage Temperature Range	T_{stg}	-65 to 150	

NOTES:1.Maximum package power dissipation limits must be observed.

2.ESD data available upon request.

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■ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, T_A = T_{low} to T_{high} [Note 3], unless otherwise specified.)

Characteristics	Symbol	Min	Typ	Max	Unit
OSCILLATOR					
Frequency ($V_{Pin\ 5}$ = 0 V, C_T = 1.0 nF, T_A = 25℃)	f_{osc}	24	33	42	kHz
Charge Current (V_{CC} = 5.0 V to 40 V, T_A = 25℃)	I_{chg}	24	35	42	μA
Discharge Current (V_{CC} = 5.0 V to 40 V, T_A = 25℃)	I_{dischg}	140	220	260	μA
Discharge to Charge Current Ratio (Pin 7 to V_{CC}, T_A = 25℃)	I_{dischg}/I_{chg}	5.2	6.5	7.5	–
Current Limit Sense Voltage (I_{chg} = I_{dischg}, T_A = 25℃)	$V_{ipk(sense)}$	250	300	350	mV
OUTPUT SWITCH (Note 4)					
Saturation Voltage, Darlington Connection (Note 5) (I_{SW} = 1.0 A, Pins 1, 8 connected)	$V_{CE(sat)}$	–	1.0	1.3	V
Saturation Voltage, Darlington Connection (I_{SW} = 1.0 A, $R_{Pin\ 8}$ = 82 Ω to V_{CC}, Forced β ≃ 20)	$V_{CE(sat)}$	–	0.45	0.7	V
DC Current Gain (I_{SW} = 1.0 A, V_{CE} = 5.0 V, T_A = 25℃)	h_{FE}	50	75	–	–
Collector Off–State Current (V_{CE} = 40 V)	$I_{C(off)}$	–	0.01	100	μA
COMPARATOR					
Threshold Voltage T_A = 25℃ T_A = T_{low} to T_{high}	V_{th}	 1.225 1.21	 1.25 –	 1.275 1.29	V
Threshold Voltage Line Regulation (V_{CC} = 3.0 V to 40 V)	Reg_{line}	–	1.4	6.0	mV
Input Bias Current (V_{in} = 0 V)	I_{IB}	–	–20	–400	nA
TOTAL DEVICE					
Supply Current (V_{CC} = 5.0 V to 40 V, C_T = 1.0 nF, Pin 7 = V_{CC}, $V_{Pin\ 5}$ > V_{th}, Pin 2 = Gnd, remaining pins open)	I_{CC}	–	–	4.0	mA

NOTES: 3. Tlow=0℃,Thigh=70℃

4.Low duty cycle techniques are used during test to maintain junctain juntion temperature as close to ambient temperature as possible.

5.If the output switch is driven into hard saturation (non-Darlington configuration)at low switch currents(≤300mA) and high driver currents(≥30mA),it may take up to 2.0 for it to come out of saturation .This condition will shorten the off time at frequencies ≥30 kHz,and is magnified at high temperatures.This condition does not occur with a Darlington configuration,sincethe output switich cannot saturare.If a non-Darlington configuration is used,the following output drive sondition is tecommended:

$$\text{Forced } \beta \text{ of output switch: } \frac{\text{IC output}}{\text{IC driver} - 7.0\text{ mA}^*} \geqslant 10$$

*The 100 Ω resistor in the emitter of the driver requires about 7mA before the output switch conducts.

■ Marking

Marking	34064

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Figure 1. Output Switch On–Off Time versus Oscillator Timing Capacitor

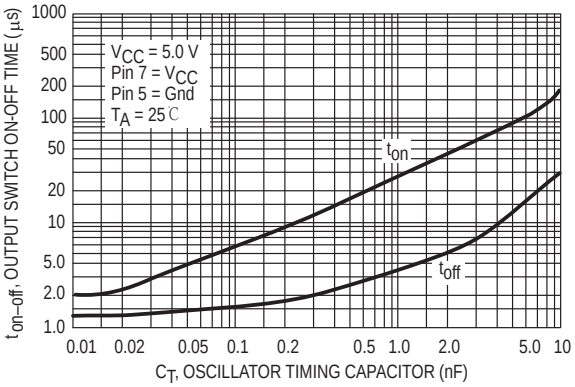


Figure 2. Timing Capacitor Waveform

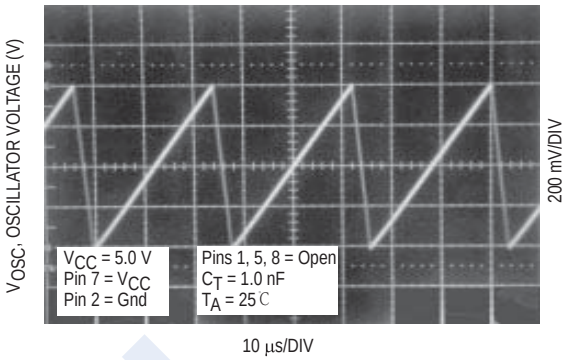


Figure 3. Emitter Follower Configuration Output Saturation Voltage versus Emitter Current

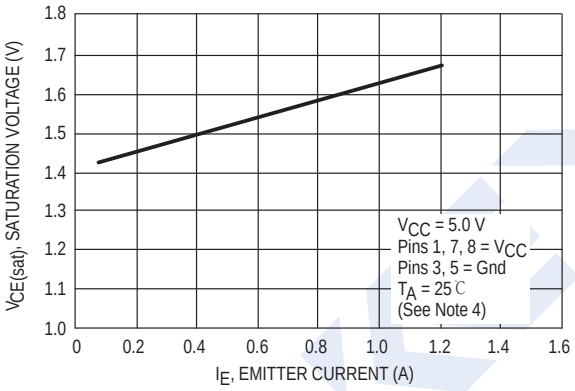


Figure 4. Common Emitter Configuration Output Switch Saturation Voltage versus Collector Current

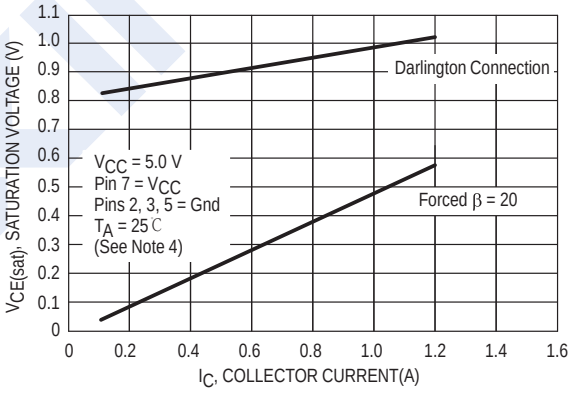


Figure 5. Current Limit Sense Voltage versus Temperature

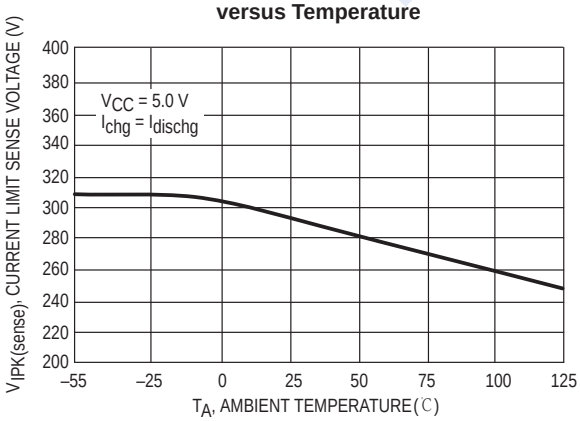
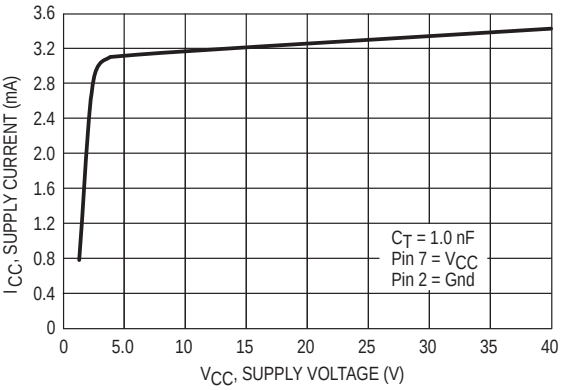


Figure 6. Standby Supply Current versus Supply Voltage



NOTE: 4. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible.

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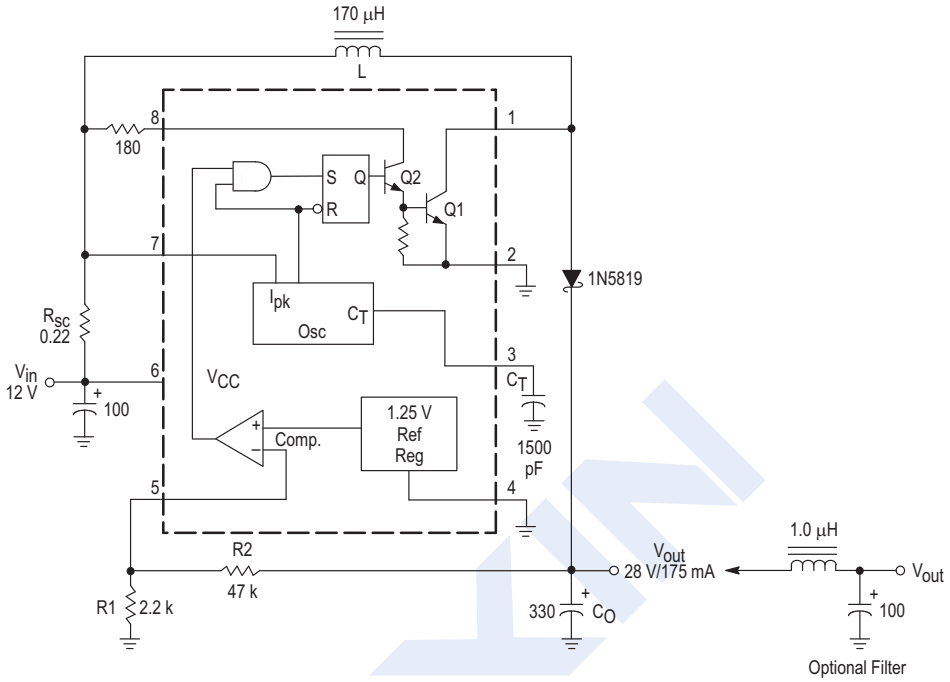
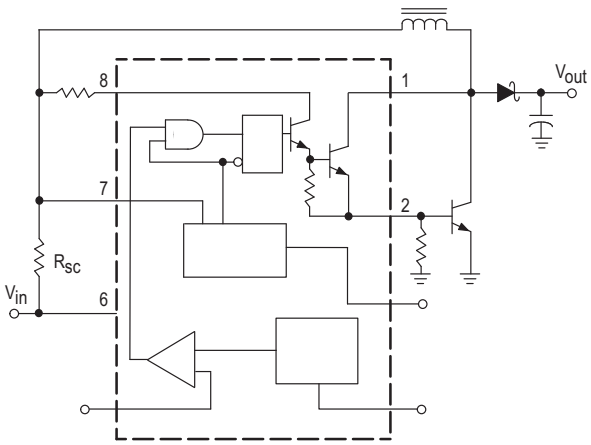
Figure 7. Step–Up Converter



Test	Conditions	Results
Line Regulation	V_{in} = 8.0 V to 16 V, I_O = 175 mA	30 mV =± 0.05%
Load Regulation	V_{in} = 12 V, I_O = 75 mA to 175 mA	10 mV =± 0.017%
Output Ripple	V_{in} = 12 V, I_O = 175 mA	400 mVpp
Efficiency	V_{in} = 12 V, I_O = 175 mA	87.7%
Output Ripple With Optional Filter	V_{in} = 12 V, I_O = 175 mA	40 mVpp

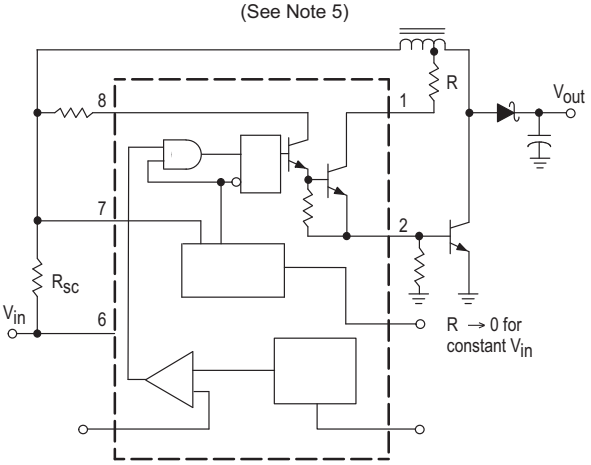
Figure 8. External Current Boost Connections for I_C Peak Greater than 1.2 A

8a. External NPN Switch



8b. External NPN Saturated Switch

(See Note 5)



NOTE: 5. If the output switch is driven into hard saturation (non–Darlington configuration) at low switch currents (≤ 300 mA) and high driver currents (≥ 30 mA), it may take up to 2.0 µs to come out of saturation. This condition will shorten the off time at frequencies ≥ 30 kHz, and is magnified at high temperatures. This condition does not occur with a Darlington configuration, since the output switch cannot saturate. If a non–Darlington configuration is used, the following output drive condition is recommended.

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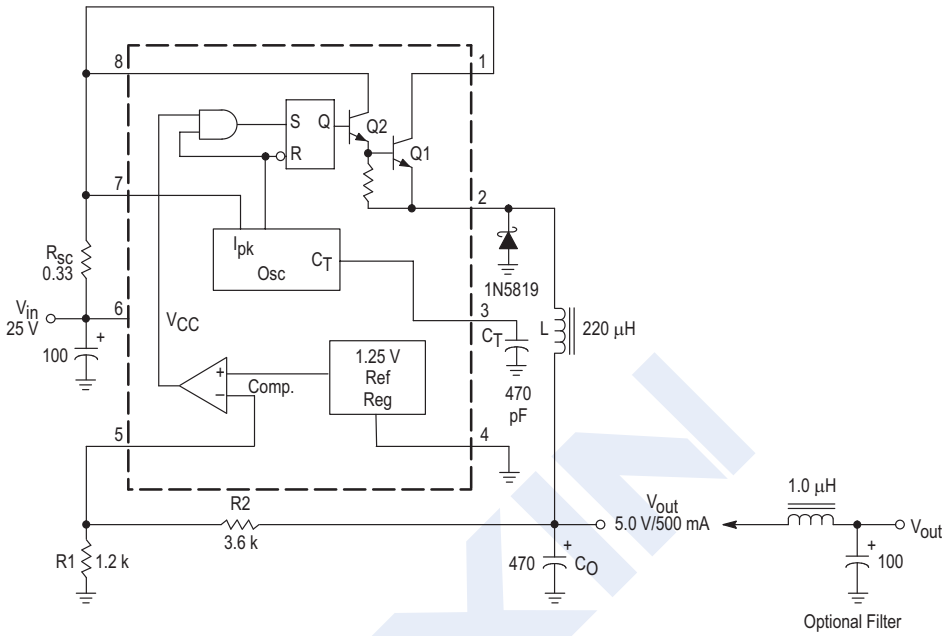
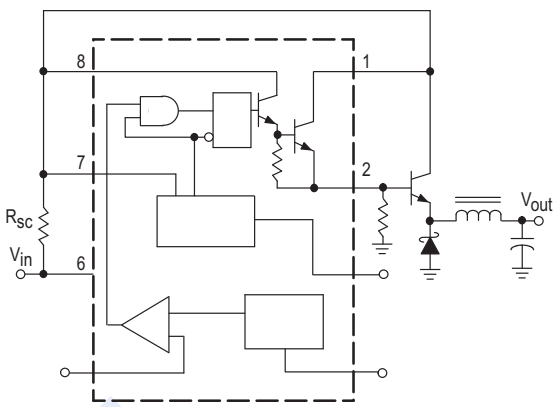
Figure 9. Step–Down Converter



Test	Conditions	Results
Line Regulation	V_{in} = 15 V to 25 V, I_O = 500 mA	12 mV =± 0.12%
Load Regulation	V_{in} = 25 V, I_O = 50 mA to 500 mA	3.0 mV =± 0.03%
Output Ripple	V_{in} = 25 V, I_O = 500 mA	120 mVpp
Short Circuit Current	V_{in} = 25 V, R_L = 0.1 Ω	1.1 A
Efficiency	V_{in} = 25 V, I_O = 500 mA	83.7%
Output Ripple With Optional Filter	V_{in} = 25 V, I_O = 500 mA	40 mVpp

Figure 10. External Current Boost Connections for I_C Peak Greater than 1.2 A

10a. External NPN Switch



10b. External PNP Saturated Switch

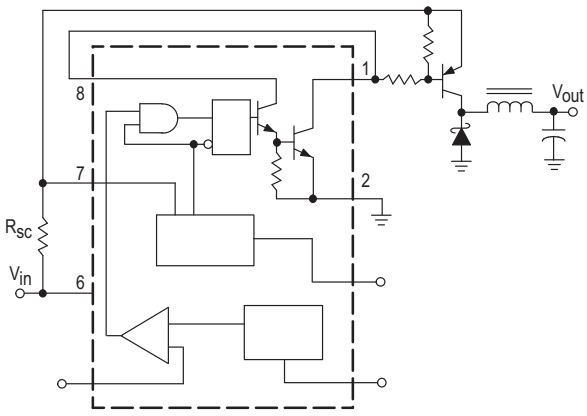


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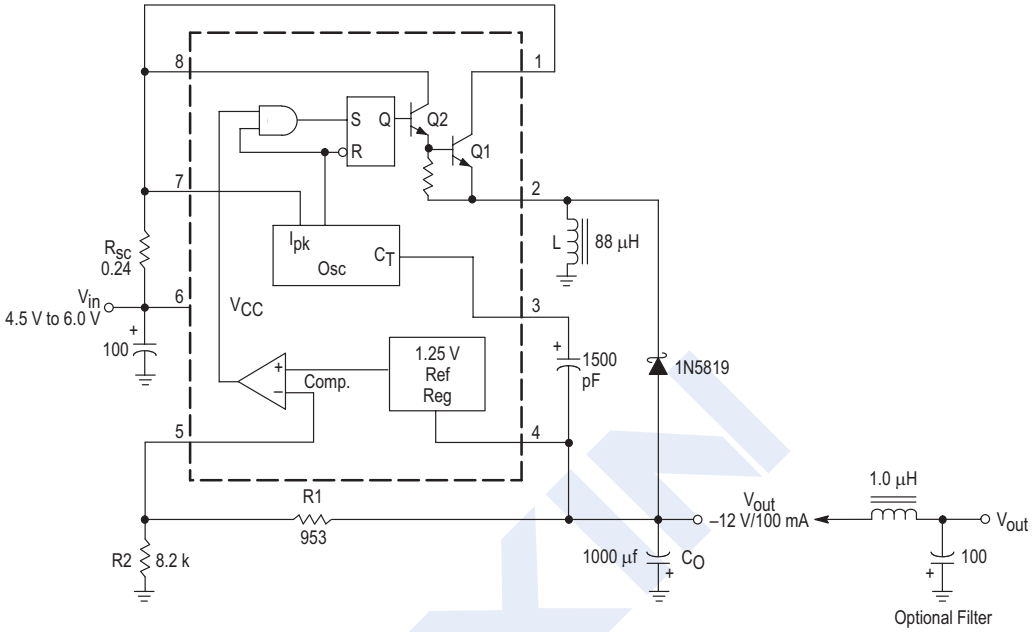
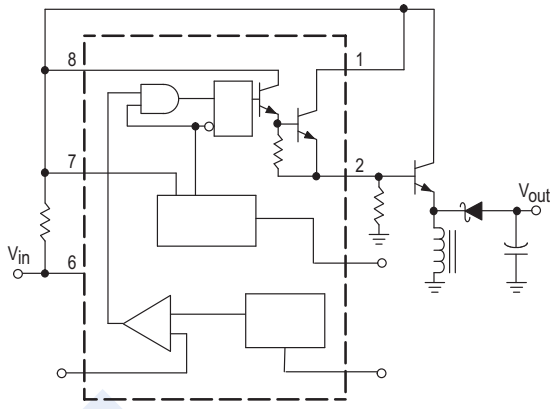
Figure 11. Voltage Inverting Converter



Test	Conditions	Results
Line Regulation	V_{in} = 4.5 V to 6.0 V, I_O = 100 mA	3.0 mV =± 0.012%
Load Regulation	V_{in} = 5.0 V, I_O = 10 mA to 100 mA	0.022 V =± 0.09%
Output Ripple	V_{in} = 5.0 V, I_O = 100 mA	500 mVpp
Short Circuit Current	V_{in} = 5.0 V, R_L = 0.1 Ω	910 mA
Efficiency	V_{in} = 5.0 V, I_O = 100 mA	62.2%
Output Ripple With Optional Filter	V_{in} = 5.0 V, I_O = 100 mA	70 mVpp

Figure 12. External Current Boost Connections for I_C Peak Greater than 1.2 A

12a. External NPN Switch



12b. External PNP Saturated Switch

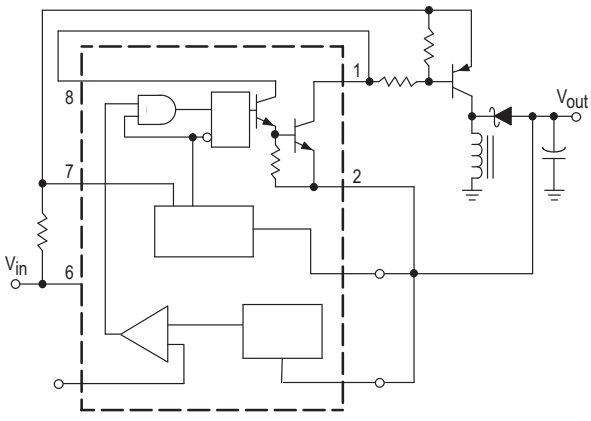


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Figure 13. Design Formula Table

Calculation	Step–Up	Step–Down	Voltage–Inverting
t_{on}/t_{off}	$\frac{V_{out} + V_F - V_{in(min)}}{V_{in(min)} - V_{sat}}$	$\frac{V_{out} + V_F}{V_{in(min)} - V_{sat} - V_{out}}$	$\frac{\lvert V_{out}\rvert + V_F}{V_{in} - V_{sat}}$
$(t_{on} + t_{off})$	$\frac{1}{f}$	$\frac{1}{f}$	$\frac{1}{f}$
t_{off}	$\frac{t_{on} + t_{off}}{\frac{t_{on}}{t_{off}} + 1}$	$\frac{t_{on} + t_{off}}{\frac{t_{on}}{t_{off}} + 1}$	$\frac{t_{on} + t_{off}}{\frac{t_{on}}{t_{off}} + 1}$
t_{on}	$(t_{on} + t_{off}) - t_{off}$	$(t_{on} + t_{off}) - t_{off}$	$(t_{on} + t_{off}) - t_{off}$
C_T	$4.0 \times 10^{-5}\, t_{on}$	$4.0 \times 10^{-5}\, t_{on}$	$4.0 \times 10^{-5}\, t_{on}$
$I_{pk(switch)}$	$2I_{out(max)}\left(\frac{t_{on}}{t_{off}} + 1\right)$	$2I_{out(max)}$	$2I_{out(max)}\left(\frac{t_{on}}{t_{off}} + 1\right)$
R_{sc}	$0.3/I_{pk(switch)}$	$0.3/I_{pk(switch)}$	$0.3/I_{pk(switch)}$
$L_{(min)}$	$\left(\frac{(V_{in(min)} - V_{sat})}{I_{pk(switch)}}\right) t_{on(max)}$	$\left(\frac{(V_{in(min)} - V_{sat} - V_{out})}{I_{pk(switch)}}\right) t_{on(max)}$	$\left(\frac{(V_{in(min)} - V_{sat})}{I_{pk(switch)}}\right) t_{on(max)}$
C_O	$9\,\frac{I_{out}t_{on}}{V_{ripple(pp)}}$	$\frac{I_{pk(switch)}(t_{on} + t_{off})}{8V_{ripple(pp)}}$	$9\,\frac{I_{out}t_{on}}{V_{ripple(pp)}}$

V_{sat} = Saturation voltage of the output switch.
V_F = Forward voltage drop of the output rectifier.

The following power supply characteristics must be chosen:

V_{in} – Nominal input voltage.
V_{out} – Desired output voltage, $|V_{out}| = 1.25\left(1+\frac{R2}{R1}\right)$
I_{out} – Desired output current.
f_{min} – Minimum desired output switching frequency at the selected values of V_{in} and I_O.
$V_{ripple(pp)}$ – Desired peak–to–peak output ripple voltage. In practice, the calculated capacitor value will need to be increased due to its equivalent series resistance and board layout. The ripple voltage should be kept to a low value since it will directly affect the line and load regulation.